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MoS_2 Homojunctions Transistors Enabled by Dimension Tailoring Strategy

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2D semiconductors present tunable property with the physical dimension. Herein, an efficient strategy to modulate the band structure of ultrathin channel by dimension tailoring of the 2D materials is reported. In order to verify the practicability of this strategy, bulk-MoS_2/MoS_2 nanoribbon (NR) homojunctions are constructed with a rectification ratio approaching up to 10^4 and an ideality factor of 1.77 which readily enable the fabrication of MoS_2-based metal-semiconductor field-effect transistors, and the bulk-MoS_2 and the MoS_2 NR serve as gate and channel, respectively. The fabricated devices exhibit robust performance, such as high saturation current of 46 $\mu A \cdot \mu m^{-1}$ and high on–off ratio over 5×10^5 at room temperature. The output current presents a high value of 140 $\mu A \cdot \mu m^{-1}$ at 77 K, then decreases with temperature. Moreover, the fabricated inverter provides a voltage gain of 15.4 and a near-ideal noise margin of 83% of supply voltage. This strategy indicates an alternative way to construct transistors based on the derivative of the same 2D material.

1. Introduction

The continued miniaturization of metal-oxide semiconductor field-effect transistors (MOSFETs) has enabled ever-increasing speed and integration density.[1,2] The ability to accurately customize its functional properties in applications is becoming increasingly important, which significantly relies on doping engineering. However, silicon-based MOSFETs require super-steep doping profiles at the drain-channel and source-channel junctions, and thus the atomic scale effects start to play dominant role in the electrical performance.[3] Although the random dopant fluctuation induced variability in MOSFETs has been mediated by introducing innovative transistor architectures that tolerate low-channel doping, such as fin field-effect transistors and fully depleted silicon-on-insulator transistors, the discreteness of charge and granularity of matter leads to purely inevitable statistical variations.[4,5] Up to date, it is challenging to eliminate random dopant fluctuation issues while miniaturization in the traditional silicon-based devices.

Moreover, to maintain desirable gate controllability and high-density integration as the continuous scaling down, the thickness of channel materials should be further decreased. However, while the silicon film thickness decreases below down to 10 nm, the line edge and surface roughness result in poor carrier mobility and high parasitic contact resistance. Notably, the atom thickness of 2D materials, such as MoS_2, offer a possible solution to fabricate ultrathin high-performance transistors, as well as the electronic circuits.[6–11] 2D materials are immune to surface roughness induced carrier scattering, which can overcome the limitation of channel thickness variation confronted by silicon-based MOSFETs. On the other hand, the lateral confinement in 2D materials has also been proved to be an effective way for band modulation.[12] For example, graphene as a zero-bandgap material, can develop measurable bandgap by cutting into nanoribbon (NR) along the certain lattice direction.[13] The previous works indicate that MoS_2 band structure can also be readily modulated by tailoring physical dimension of MoS_2 NR, because of the quantum confinement effect. Conversely with graphene, the bandgap scaling of MoS_2 is proportional to the NR width as the theoretical prediction.[14,15]

In this paper, by tailoring the physical dimension of MoS_2 NR, the band structure can be experimentally tuned. The bulk-MoS_2/MoS_2 NR homojunctions with abrupt energy level

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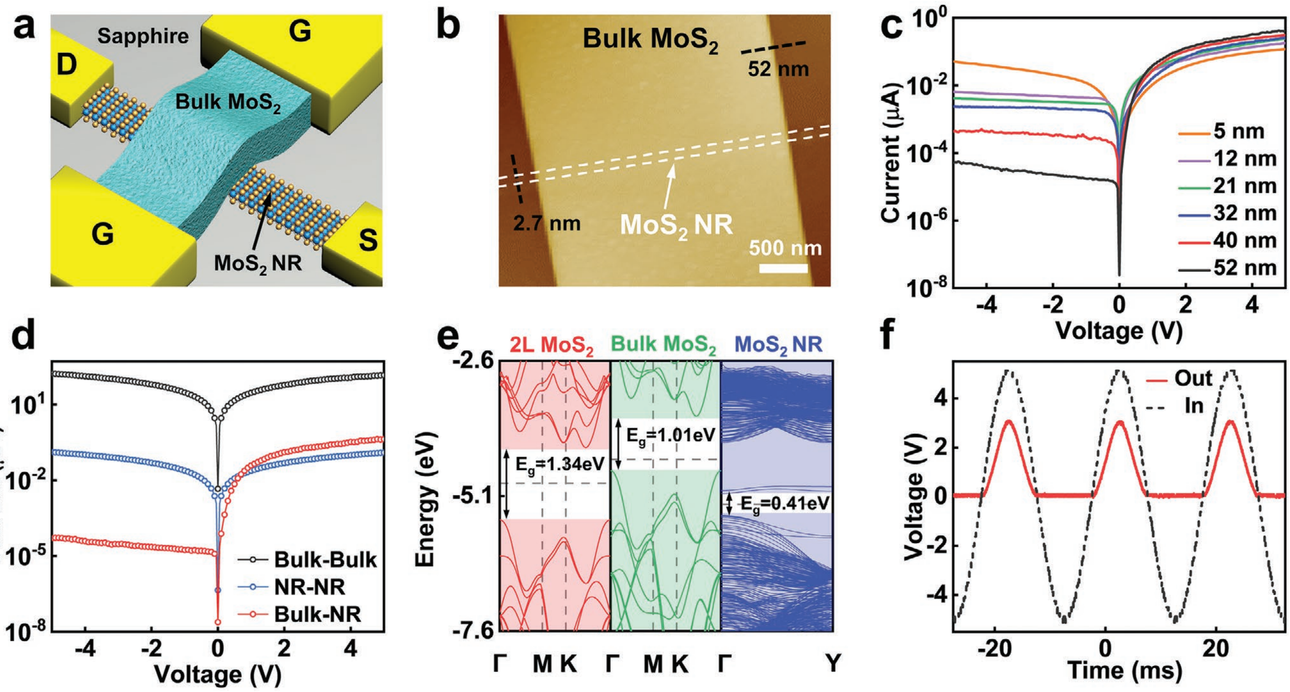

Figure 1. Electrical performance of the bulk-MoS_2/MoS_2 nanoribbon (NR) homojunctions. a) Schematic illustration of MoS_2 MESFETs, fabricated on sapphire substrate. b) Atomic-force microscopy (AFM) image of the bulk-MoS_2/MoS_2 NR homojunction. c) Evolution of the rectification characteristics of the MoS_2 homojunction with varied thicknesses of the bulk-MoS_2. d) Current–voltage curves of bulk-MoS_2 nanosheet, MoS_2 NR channels, and the bulk-MoS_2/MoS_2 NR homojunction. e) Density functional theory (DFT) calculated band structures of bilayer (2L) MoS_2, bulk-MoS_2, 2L MoS_2 based on the for the non-close-contact model. f) Dynamic rectification of the bulk-MoS_2/MoS_2 NR homojunction.

change are constructed, and present an ideality factor of 1.77 and a high rectification ratio of ≈10^4. By using the bulk-MoS_2 and the MoS_2 NR as gate and carrier transportation channel, respectively, MoS_2 metal-semiconductor field-effect transistors (MESFETs) are fabricated. The MESFETs present negligible gate hysteresis with subthreshold swing (SS) down to 120 mV·dec^{-1}. In addition, the device shows robust performance with high on-state current of 46 μA·μm^{-1}, threshold voltage (V_{TH}) of –1.08 V, and property of easy saturation. Compared with the previously reported 2D-heterojunction MESFETs, the MoS_2 MESFETs not only avoids uncontrollable intrinsic doping processes, but also are compatible with existing technology.[16–18] An inverter based on MoS_2 MESFET is assembled on sapphire substrate, which presents a voltage gain of 15.4 and a near-ideal noise margin of 83% of supply voltage. Therefore, the proposed strategy opens up possibilities for fabricating transistors based on derivatives from the same materials.

2. Results and Discussions

Figure 1a shows the schematic image of the MoS_2 MESFETs fabricated on a sapphire substrate, by constructing the bulk-MoS_2/MoS_2 NR homojunctions. Briefly, the MoS_2 NR is obtained by argon plasma etch (Experimental Section), and then the bulk-MoS_2 is transferred via a dry physical approach. The contact and gate regions are defined by e-beam lithography (EBL), followed by metal deposition and lift-off processes. Typical atomic-force microscopy (AFM) image of the MESFET is presented in Figure 1b. The thickness of the MoS_2 NR channel is measured to be 2.7 nm, and the bulk-MoS_2 gate is in 52 nm thick. Figure 1c shows the rectification characteristics of the bulk-MoS_2/MoS_2 NR homojunctions with varying bulk-MoS_2 thickness. Due to the poor conductivity and edge defects induced by scattering effect, the devices with monolayer MoS_2 NR present poor on–off ratio and on-state current. As the bulk-MoS_2 thickness increases, the on–off ratio increases correspondingly and yields a peak value of 10^4. In other words, the rectification characteristics of the bulk-MoS_2/MoS_2 NR homojunction degrade as the thickness of the bulk-MoS_2 decreases. With the thickness of the bulk-MoS_2 scaling down to 5 nm, the epibiotic rectification characteristics indicate that the dimension tailoring can efficiently modulate the band structure of MoS_2 NR.[19] To further state the rectification characteristic is originated from the homojunctions, the transportation of the bulk-MoS_2, MoS_2 NR and bulk-MoS_2/MoS_2 NR homojunction are measured, as shown in Figure 1d. The bulk-MoS_2 presents low resistance of 7.4 Ω·cm^{-1}. The individual MoS_2 NR channels present a high resistance, which can be attributed to carrier scattering and induced by the linewidth roughness introduced by argon plasma etching process.[20] Hence, the electrical performance of the homojunction can be further improved by introducing advanced etching techniques. Notably, both the bulk-MoS_2 and the MoS_2 NR show linear conductance, indicating the formation of quasi-ohmic contact.[21] Typical electrical characteristics of multilayered MoS_2/bulk MoS_2 homojunction are shown in Figure S1, Supporting Information. Specially, ideal rectification is observed in the bulk-MoS_2/MoS_2

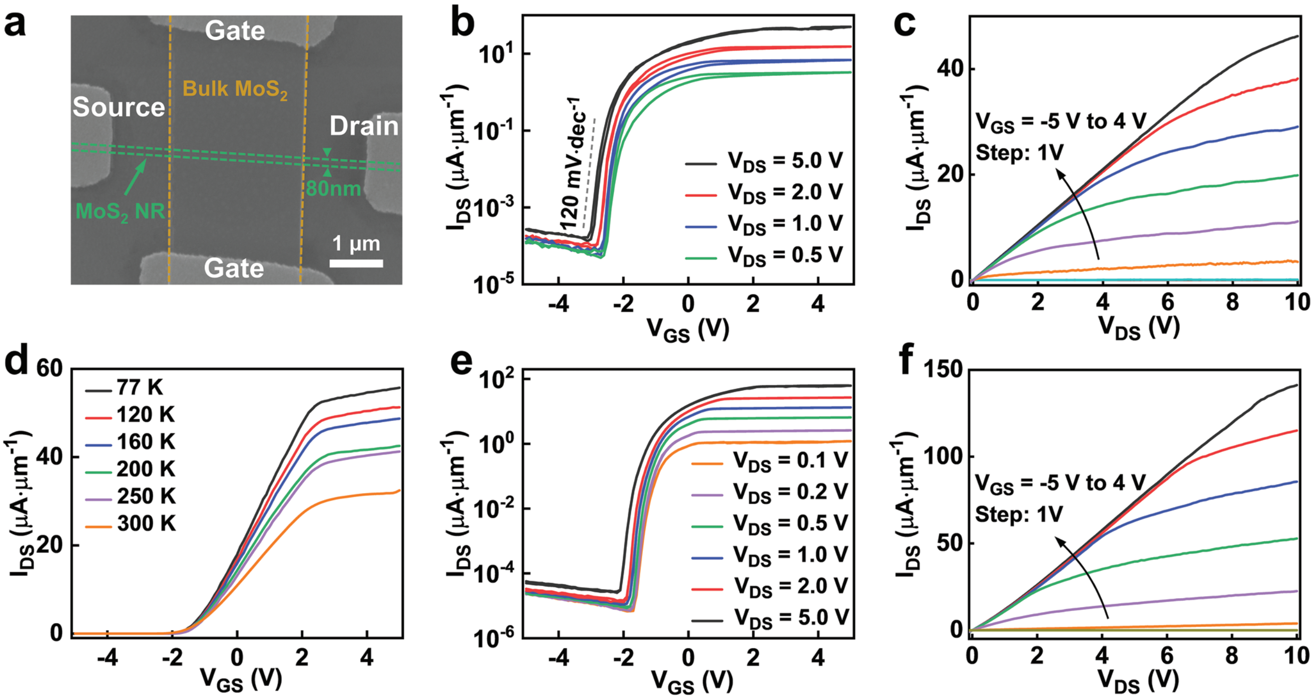

Figure 2. Electrical performance and low temperature characteristics of MoS_2 MESFET on sapphire substrate. a) Scanning electron microscope (SEM) of MoS_2 MESFET. b) Typical transfer characteristics at different V_{DS}. c) Output curves of the MoS_2 MESFETs at varied V_{GS} from −5 to 4 V. d) Transfer characteristics of MoS_2 MESFET at V_{GS} = 5 V with different temperatures. e) Typical transfer characteristics with different V_{DS}, at 77 K. f) Output curves of the MoS_2 MESFET at V_{GS} = −5 V to V_{GS} = 4 V, at 77 K.

NR, which shows an ideality factor of 1.77 (Figure S2, Supporting Information) and a rectification ration of 10^4. To state the reason of the evolution of electrical performance of MoS_2 homojunctions, the density functional theory (DFT) is performed (Experimental Section). As shown in Figure 1e, the extracted E_g values are 1.34, 1.01, and 0.41 eV for bilayer (2L) MoS_2, bulk-MoS_2, and 2L MoS_2 NR, respectively. Notably, the Fermi level pinning of elemental metals, close to the conduction band, leads to large barrier heights for holes with limited hole injection from the contacts, and thus the NR present n-type characteristics, while the DFT results indicated p type characteristic.[22] Dynamic rectifying of the bulk-MoS_2/MoS_2 NR homojunction is demonstrated in Figure S3, Supporting Information. In Figure 1f, a sinusoidal input waveform of peak-to-peak value of 5 V at 50 Hz is applied; due to the high parasitic resistance in the MoS_2 NR, a fidelity output signal with 3 V is observed, indicating superior rectifying performance of the diode.[23,24] Therefore, the depletion region at the bulk-MoS_2/MoS_2 NR homojunction hinders a significant gate leakage current and can readily perform the function of local gate in MoS_2 MESFETs.

Compared with traditional MOSFETs, MESFETs are free of complex dielectric deposition processes. Their gate voltage controls the barrier height to alter the depletion region width of the channel, which leads to the on and off states of the channel. This structure can efficiently avoid dielectric deposition challenges in 2D materials transistors. **Figure 2**a displays a scanning electron microscope (SEM) image of MoS_2 MESFETs with a channel length is 4.5 µm. The green dotted line indicates the 80 nm-wide MoS_2 NR channel. The MoS_2 NR width is limited by diameter of the etch mask. However, as the channel width decreases below 80 nm, the edge roughness and defects on the MoS_2 NR dominate the carrier transport in the channel, resulting in inferior electrical performance, as shown in Figure S4, Supporting Information. The electrical transportation mechanism of the MoS_2 MESFETs is schematically illustrated in Figure S5, Supporting Information. With a positive gate voltage applied, the depletion region is shrunk and then the MoS_2 NR channel is turned on. With a negative gate voltage applied, the depletion region is expanded until the channel is fully depleted. Figure 2b is the semi-log plot of the transfer characteristics at different drain-to-source voltages (V_{DS}). The high on–off ratio over 5×10^5 proves a great gate control ability of the bulk-MoS_2 local gate. Considering the static power consumption of transistors, we obtain a low V_{TH} about of −2 V and the characteristics of easy saturation are observed.[25,26] The van der Waals interface of MoS_2 MESFETs possesses low-density traps, leading to negligible hysteresis and a low SS of 120 mV·dec^{-1} at room temperature.[27] Moreover, the gate leakage (I_g) current is about 10 pA (Figure S6, Supporting Information). A high output current density of 46 µA·µm^{-1} is obtained, as shown in Figure 2c. Due to the poor conductivity and edge defects induced by scattering effect, the devices with monolayer NR obtain poor on–off ratio and on-state current (Figure S7, Supporting Information). In order to further study the temperature effect on electrical characteristics of MoS_2 MESFETs, the I_{DS}–V_{GS} curves are obtained at varied temperatures from 77 to 300 K. As shown in Figure 2d, I_{DS} decreases with increasing temperature and tend to saturate under a large V_{GS}, which can be mainly ascribed to the enhanced scattering with temperature or the release of

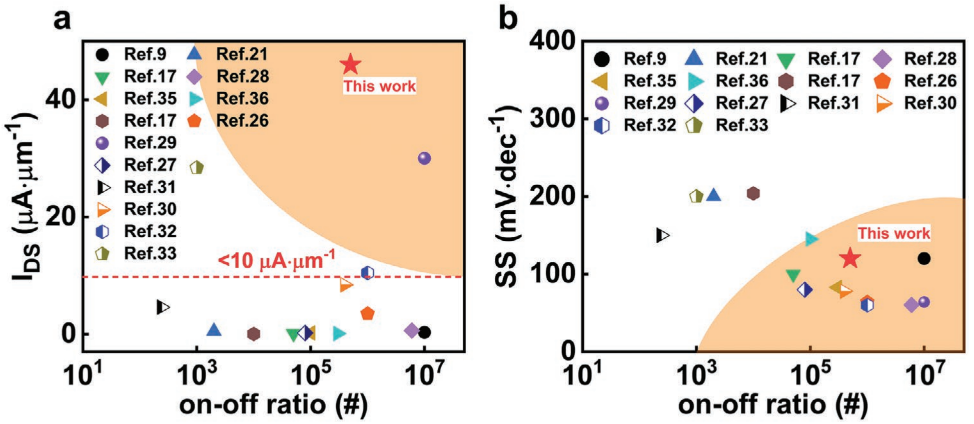

Figure 3. Comparison of different important parameters of similar structures. a) Comparison of maximum output current density and on–off ratio. b) Comparison of SS and on–off ratio.

trapped electrons at the interface.[28] In Figure S8, Supporting Information, the V_{TH} of MoS_2 MESFETs shifts to negative values and I_{DS} decreases as temperature increases, finally showing a low V_{TH} of –1.08 V at 77 K. Figure 2e shows typical transfer characteristics of MoS_2 MESFETs with various V_{DS} from 0.1 to 5.0 V at 77 K, indicating improved on-state current, and off-state current maintains a relative low level. In Figure 2f, the maximum output current of 140 $\mu A \cdot \mu m^{-1}$ can be achieved at $V_{GS} = 4.0$ V at 77 K.

The maximum output current density and on–off ratio of the previously reported 2D-based MESFETs are compared in **Figure 3**a. The current density of the devices is in the range of 1–10 $\mu A \cdot \mu m^{-1}$. Although several optimized devices select 1D nanowires channel or self-alignment technique can achieve high current density,[29–33] the current density value distributes below 30 $\mu A \cdot \mu m^{-1}$. In this work, by geometric tailoring the dimension of MoS_2, the devices based on the bulk-MoS_2/MoS_2 NR homojunctions have achieved a high current density of 46 $\mu A \cdot \mu m^{-1}$, which is about 40 times higher than the reported 2D-based junction field-effect transistors or MESFETs. MoS_2 NRs can effectively confine the device current in a narrow 1D region to suppress the electron scattering effectively, therefore, a high current density is achieved. In order to further evaluate the device performance and power consumption, SS and on–off ratio are illustrated in Figure 3b. In general, on–off ratio above 10^3 is the prerequisite to realize high-performance digital logic devices. On the contrary, the SS beyond 200 $mV \cdot dec^{-1}$ will lead to a sharp increase in power consumption. The devices in this work can offer superior current drivability than the reported ones, with only a small sacrifice in terms of on–off ratio and SS, indicating an excellent trade-off among the key parameters.

Direct-coupled field-effect transistor logic (DCFL) technology is a popular architecture and is highly suitable for the low-power 2D electronics.[34,35] Based on DCFL technology, the NOT gate inverter is constructed, as shown in **Figure 4**a. Figure 4b exhibits the voltage transfer characteristics of the inverter with different supply voltages (V_{DD}), where V_{OUT} and V_{IN} are output and input voltages, respectively. Figure 4c shows the voltage gain of the inverter with different V_{DD}. As the V_{DD} increases, the voltage gain increases and correspondingly yields a peak value of 15.4 at $V_{DD} = 1$ V. As shown in Figure 4d, we extract the high noise margin (NM_H) and low noise margin (NM_L) from the voltage transfer characteristics and its specular reflection curve.[36,37] It shows that $NM_L = 0.424\ V_{DD}$ and $NM_H = 0.405\ V_{DD}$ are obtained at $V_{DD} = 1$ V, indicating the robustness of the inverter noise with a total noise margin of 83%. Hence, a proof-of-concept demonstration of the MoS_2 MESFETs-based logic circuit is implemented by assembling an inverter.

3. Conclusion

In conclusion, this work proposes an effective strategy to tune the band structure of ultrathin 2D materials. Electrical performance of bulk-MoS_2/MoS_2 NR homojunctions and DFT calculation indicate the feasibility of dimension tailoring strategy. Benefiting from the abrupt changed band structure of MoS_2 homojunctions, the MoS_2 MESFETs exhibit robust performance with high output current, negligible hysteresis, low SS, and high on–off ratio. Meanwhile, the assembled inverters present desirable electrical performance. Therefore, the proposed strategy provides an advanced way to tune the band structure of 2D materials for advanced logic electronics.

4. Experimental Section

Device Fabrication: MoS_2 flakes were mechanically exfoliated from a bulk crystal (SPI company) by using Scotch tape and thereafter transferred to the pretreated sapphire substrate. Subsequently, the Ga_2O_3 nanowires were transferred onto the preprepared MoS_2 flakes via the dry transfer technique. Ga_2O_3 nanowires were employed as an etch mask. Ga_2O_3 nanowires were synthesized by a typical chemical vapor deposition method in a single zone horizontal tube furnace. 300 nm SiO_2/p^+-Si substrate coated with 0.8-nm Au was served as the growth substrate, and it was covered onto the quartz boat with the Ga_2O_3 powder/carbon source (weight ratio of 10:1). After 20 min of purging, the furnace was heated up to 1050 °C for 30 min with an O_2/Ar mixed gas (volume ratio of 1:99) and rate of 200 sccm, then cooled down to room temperature naturally. Through argon plasma etching and subsequent removal the residue of Ga_2O_3 nanowires by ultrasonic, a MoS_2 NR was prepared. The MoS_2 NR geometry was formed with a etch rate of 15 $nm \cdot min^{-1}$. Next, a 50 nm-thick MoS_2 flake was transferred to the preprepared MoS_2 NR by aligned transfer platform. Finally,

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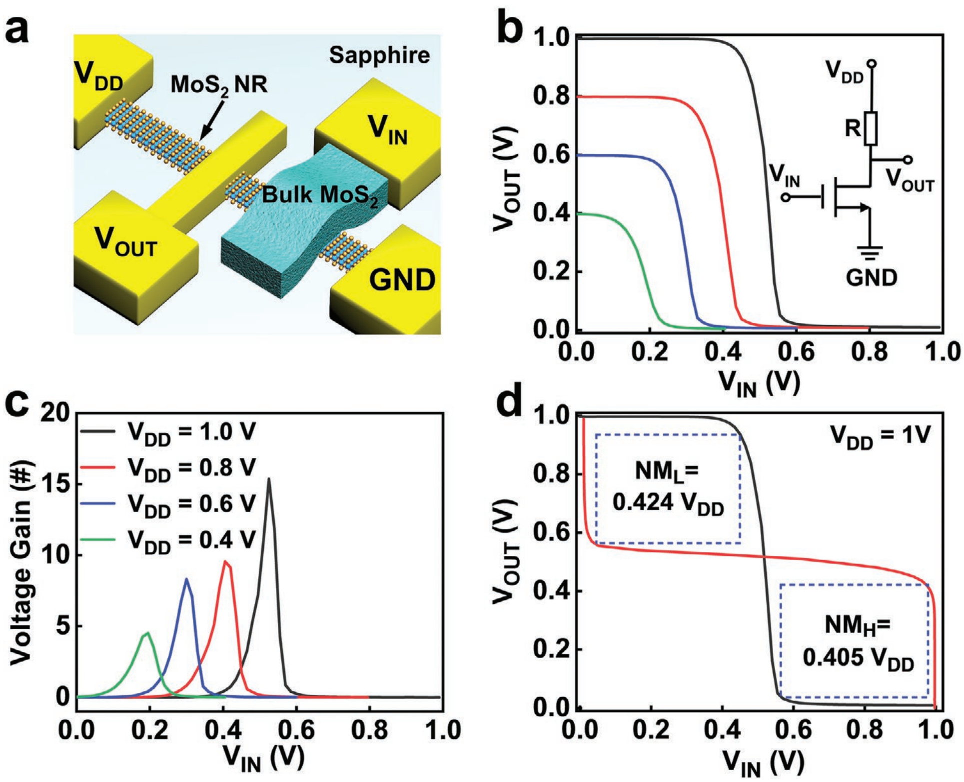

Figure 4. Electrical performance of the inverter based on MoS_2 MESFETs. a) Schematic illustration of the inverter on sapphire substrate. b) Voltage transfer characteristics of the inverter at different V_{DD}. The insets present the schematic image of circuit for inverter. c) Voltage gain of the inverter. d) Noise margins ($NM_L = 0.427\ V_{DD}$, $NM_H = 0.405\ V_{DD}$) of the inverter at $V_{DD} = 1$ V.

gate/source/drain region were defined by EBL technology, and the Cr/Au (10/50 nm) electrode was deposited by thermal evaporator after the lift-off process.

Materials Characterization and Electrical Measurements: The morphology of the homojunction was characterized by SEM (JEOL IT300) and AFM (Park NX20). Electrical measurements were carried out by employing a Lakeshore TTPX probe station and Agilent B1500A semiconductor parameter analyzer.

Density Functional Theory Computational Methods: DFT calculations were performed based on first-principles methods, which were implemented in the Vienna ab initio simulation package. The electron-ion potential and exchange–correlation functional were described by the projector-augmented wave method and the generalized gradient approximation in the scheme of Perdew–Burke–Ernzerhof parameterization, respectively. The vacuum space interval was set to be 20 Å in both edge-to-edge and layer-to-layer directions, which was large enough to separate the van der Waals interaction between adjacent images and satisfied the Bloch periodic boundary conditions in the rest dimension. Energy cut off value was set to be 500 eV. The structures were fully relaxed until the Hellmann-Feynman forces acting on each atom were less than 0.01 eV $Å^{-1}$ and the total energy was converged to 10 to 5 eV. The DFT-D3 method was applied for the van der Waals interactions in all simulations. Armchair MoS_2 NRs passivated with H atoms and width $N_a = 48$ was used to perform the calculations (N_a was defined as the number of dimmer lines across the NR width). For NRs, Brillouin zone was sampled by 25 × 1 × 1 k-points.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

dimension tailoring, homojunctions, inverters, transistors

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